REMARKS

Applicants have amended their abstract in light of the objection thereto, in Item 2 on page 2 of the Office Action mailed November 20, 2008. Specifically, Applicants respectfully traverse the objection to the abstract "because extensive mechanical and design details of apparatus should not be given", as contended by the Examiner. It is respectfully submitted that the present invention involves use of specific apparatus, and it is respectfully submitted that the disclosure of the apparatus used is clearly appropriate in the present abstract.

The request by the Examiner to delete reference numbers from the abstract is noted, and this suggestion has been followed in the present amendments to the abstract.

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claim 18 to incorporate therein the subject matter of claim 21; and to also recite a step of securing the IC element held be the IC element holding part with a temporary securing pin, as described on pages 20 and 21 of Applicants' specification, for example. In light of amendments to claim 18, claims 19 and 21 have been cancelled without prejudice or disclaimer, and claims 20 and 22-24 have been amended.

Entry of the present amendments is clearly proper, in view of the concurrent filing of the RCE Transmittal, the present amendments constituting the necessary Submission under 37 CFR 1.114 for the RCE.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed November 20, 2008, that is, the teachings of the U.S. patent documents to Usami, et al., Patent No. 7,036,741, to Yamakawa, Patent No. 6,479,777, to Moskowitz, et al.,

Patent No. 5,528,222, and to Green, et al., Patent Application Publication No. 2003/0136503, under the provisions of 35 USC 102 and 35 USC 103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a manufacturing method for an electronic device that has IC elements, as in the present claims, including, inter alia, wherein the method includes a step of positionally aligning the connection surfaces of the IC elements and either one of the circuit layers while continuously supplying the IC elements individually into an IC element transport mechanism, and wherein the step of continuously supplying the IC elements includes, inter alia, a step of securing the IC element held by the IC element holding part at any of the circuit layers with a temporary securing pin. See claim 18.

By providing s step of positionally aligning the connection surfaces of the IC elements and either one of the circuit layers while continuously supplying the IC elements individually into an IC elements transport mechanism, as in claim 18, a plurality of individual IC elements can be directly and simultaneously transported, positionally aligned and secured individually, so that securing on tapes or extracting from tapes, such as tape automated bonding, is not necessary, whereby effective productivity and low costs are realized.

By performing the step of securing the IC elements utilizing the temporary securing pin, the held IC elements can be extracted easily and efficiently, and immediately secured on the lower circuit layers after positionally aligning the IC elements.

According to the present invention, utilizing features as discussed previously, positional alignment and securing are performed while the IC elements are held at the holding part, so that the securing can be done with a desired accuracy when the IC elements are separated, and securing with desired accuracy can be achieved

even where the IC elements are very thin, for example, a thickness of less than 0.5 mm. Moreover, the presently claimed process can easily transport a plurality of minute, thin and separated IC elements, positionally align them individually and secure the elements on a circuit layer, so that effective productivity and low costs are realized.

Furthermore, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such a manufacturing method as in the present claims, having features as discussed previously in connection with claim 18, and, additionally, wherein the step of continuously supplying the IC elements includes a step of individually holding an IC element in an IC element holding part of a transport mechanism, which is a disc shaped IC elements transport mechanism (see claim 20), or is formed as a notch shape (see claim 21).

In addition, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such a manufacturing method as in the present claims, having features as discussed previously in connection with claim 18, and, additionally, wherein the step of continuously supplying the IC elements includes a step of aligning the IC elements by action of an IC elements alignment/supply mechanism to facilitate individually holding the IC element in the holding part (note claims 22-24), in particular, wherein the IC elements alignment/supply mechanism is a line feeder (see claim 23) or is a high frequency alignment feeder (see claim 24).

Moreover, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a manufacturing method as in the present claims, having features as discussed previously in connection with claim 18, and, additionally, having further features as in the remaining dependent claims, including (but not limited to) wherein the electrical

connection of an electrode and at least one of the circuit layers is made via an anisotropic conductive adhesive layer (see claim 25); and/or wherein the method further includes connecting, at once, the electrodes of the IC elements and at least one layer from among the first and second circuit layers, with the step of connecting being performed after the step of positionally aligning the connection surfaces (see claim 26), in particular, wherein the electrode of the IC elements and the at least one layer from among the first and second circuit layers are connected by thermal compression (see claim 27), with gaps between the first and second circuit layers being sealed by the thermal compression (see claim 28); and/or wherein the method further includes a step of cutting a continuum of the plurality of IC elements into individual pieces, with the step of cutting being performed after the connecting step (see claim 29); and/or wherein a conductive layer is formed on the surface of at least one from among the first and second circuit layers (see claim 30); and/or wherein the first and second circuit layers include aluminum (see claim 31); and/or base substrate material supporting at least one of the first and second circuit layers, as in claims 32 and 33; and/or thickness of the anisotropic conductive adhesive layers, as in claim 34.

The present invention is directed to a method of manufacturing an electronic device, illustrated (but not limited to) by a noncontact type individual identification device having IC elements.

In recent years, individual identification systems that employ radio frequency identification tags have been considered; such systems include an external antenna attached to IC elements, which enables communication to be performed over several meters. One type of such system is a TCP (Tape Carrier Package) inlet, employing a tape automated bonding method in which IC elements having all external

electrodes formed on the same surface thereof are mounted, each individually, on a tape carrier formed of a polyimide substrate.

As described in the first full paragraph on page 3 of Applicants' specification, other inlet structures include IC elements in which the external electrodes of the IC elements are formed individually on both of a pair of opposite surfaces of the IC element. The IC elements in this proposed structure have, respectively, two external electrodes formed individually on the surfaces of the IC elements, and are furnished with an excitation slit type dipole antenna, the external electrodes formed individually on each of the surfaces of the IC elements being disposed between the legs of an antenna to manufacture a sandwich antenna construction.

However, various problems arise in connection with previously proposed inlet structures and methods of manufacture thereof, as described on pages 4 and 5 of Applicants' specification. Thus, it is still desired to provide a manufacturing method for manufacturing a semiconductor device which can be utilized in an identification system, which can manufacture the device at low cost and with superior productivity, and wherein the device has satisfactory communication properties.

Against this background, Applicants achieve the foregoing objectives by the present method, including, inter alia, wherein each IC element has electrodes formed respectively on the respective surfaces of a pair of opposed sides of the IC element, with a slit being formed in the first or second circuit layer, with connecting parts electrically connecting the respective electrodes with the first and second circuit layers, and with the first and second circuit layers being connected so that the connecting parts of the first and second circuit layers are connected spanning the slit, the IC elements individually being continuously supplied into an IC elements transport mechanism in positionally aligning the connection surfaces of the IC elements and one of the first and second circuit layers.

By continuously supplying the IC elements individually into an IC elements transport mechanism as in the present claims, in particular, into a notch at the periphery of a disc shaped transport mechanism, a plurality of IC elements up to a maximum number equivalent to the number of, e.g., notches, can be simultaneously delivered, even when the delivered IC elements are arranged individually on the second circuit layer and the antenna circuits, so that superior productivity can be realized in comparison to the case where the IC elements are held by suction using a vacuum suction device or the like, and delivered and arranged one by one. As increased productivity is realized, available operating time per inlet device is reduced. Note the first full paragraph on page 16 of Applicants' specification.

By forming the connecting structure (that is, the first through third connecting parts, particularly the second and third connecting parts) spanning the slit, high precision positional alignment of the external electrode on that surface of the IC elements that is on the side in contact with the antenna circuit, with the excitation slit on the antenna circuit, is not necessary, thus reducing costs associated with manufacturing equipment and facilitating high-speed delivery of the IC elements. See page 16, lines 13-18, of Applicants' specification.

By providing electrical connections of the electrodes with the first and second circuit layers via an anisotropic conductive adhesive layer, as in, for example, claim 25, it is not necessary to have a surface coating over the antenna circuits, and there is no need to use a highly heat resistant base substrate, making it possible to use an inexpensive base material and antenna circuit, thereby enabling cost reductions. Note the paragraph bridging pages 16 and 17 of Applicants' specification.

In particular, as the IC elements are accommodated individually, e.g., in notches in the IC elements transport mechanism, with a plurality of notches arranged

circumferentially around the outside of a disc shaped transport mechanism, a maximum number of IC elements equivalent to the number of notches can be simultaneously delivered, providing improvement in the productivity. Note the last full paragraph on page 18 of Applicants' specification.

Usami, et al. discloses a technique effectively applied to a structure of a wireless IC chip used to identify an object in a non-contact manner, an IC tag for wirelessly sending an identification number, a transponder, or the like. The device has electrodes formed on front and rear surfaces of an IC chip for wirelessly transmitting/receiving data, first and second conductors being connected respectively to the electrodes. The first and second conductors include a slit, and the first and second conductors are connected to each other. See column 3, lines 58-64; note also column 3, lines 50-57; and column 4, lines 11-26. Note also column 5, lines 52-56, describing that the conductors are attached to each other with anisotropic conductive adhesive. Note column 10, lines 54-58; and column 11, lines 25-30. Note, further, column 17, lines 46-50.

It is respectfully submitted that Usami, et al. would have neither disclosed nor would have suggested such procedure as in the present claims, of positionally aligning the connection surfaces of the IC elements and either one of the circuit layers while continuously supplying the IC elements individually into an IC elements transport mechanism, as in claim 18. In connection therewith, the Examiner contends on page 4, lines 1-4, of the Office Action mailed November 20, 2008, that Usami, et al. discloses such step of positionally aligning, referring to Fig. 15A of this reference, together with column 18, lines 33-42. Such contention by the Examiner is respectfully traversed. It is respectfully submitted that Fig. 15A of Usami, et al. discloses positional alignment between a tape that mounts IC chips and another tape that has circuit layers, by use of the sprockets formed on each tape. It is respectfully

submitted that this disclosure in Usami, et al., as relied upon by the Examiner, does not teach, nor would have suggested, positional alignment between individual IC elements themselves, and circuit layers.

Moreover, it is respectfully submitted that the positional alignment using sprockets, as in Usami, et al., requires tape automated bonding, and it is respectfully submitted that Usami, et al. would have neither disclosed nor would have suggested handling separated IC elements, as achieved by the present invention.

Furthermore, it is respectfully submitted that Usami, et al. would have neither taught nor would have suggested other features of the present invention as in claim 18, including, inter alia, securing the IC element held by the IC element holding part with a temporary securing pin. It is respectfully submitted that Usami, et al. discloses use of a vacuum absorber that attaches IC chips on the second conductor by airflow, referring to Fig. 7 and a corresponding description in column 12, lines 23-26 of Usami, et al. However, a configuration that held IC elements are temporarily secured on circuit layers with a temporary securing pin would have neither been disclosed nor suggested by Usami, et al. By using airflow to attach IC chips on the second conductor, as in Usami, et al., accurate positional alignment is not obtainable. Moreover, use of a vacuum absorber to suck and transport the large number of IC chips simultaneously using a plurality of sucking sets requires a complex facility and large-scale plant investments, so that low-cost production becomes difficult. Such problems are avoided by the present invention, using the temporary securing pin.

It is respectfully submitted that the teachings of the secondary references as applied by the Examiner would not have rectified the deficiencies of Usami, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Yamakawa discloses a conveying apparatus that conveys electronic parts such as chip-type capacitors and resistors, and a method of use thereof. This patent discloses use of a conveying table which is rotationally driven in a constant direction, the table including a plurality of concave storage slots formed with identical pitches on the entire outer-peripheral section of the table. These slots store chip-type electronic parts, each slot having a bottom surface, two radial side surfaces, and an inner-circumferential side surface. Further, an air hole is provided, having one end open on the inner-circumferential side surface and the other end communicating with a negative air pressure source generating negative suction air pressure that sucks the electronic part onto the inner-circumferential side surface of the concave storage slot. The electronic part is vacuum-suctioned by negative air pressure provided through the air hole onto the concave storage slot. See column 2, lines 1-19; note also column 2, lines 52-60.

It is emphasized that Yamakawa pushes the IC chips in the tangential direction, and is unable to positionally align so as to place the IC chips at a desired position on the circuit layers with accuracy. Even combining the teachings of Usami, et al. and Yamakawa, such combined teachings would have neither disclosed nor would have suggested the presently claimed manufacturing method as in all of the present claims, including, inter alia, the step of positionally aligning the connection surfaces of the IC elements and either one of the circuit layers while continuously supplying the IC elements individually into an IC element transport mechanism.

Furthermore, it is respectfully submitted that the combined teachings of Usami, et al. and of Yamakawa would have neither taught nor would have suggested other features of the present invention, including, inter alia, securing the IC element held by the IC element holding part at any of the circuit layers with a temporary securing pin. It is respectfully submitted that the apparatus set forth in Yamakawa,

and use of such apparatus in the process of Yamakawa, supplies IC chips using airflow. It is respectfully submitted that such technique requires relatively thick IC chips, for example, the thickness of the IC chip is required to be not less than 0.5 mm in Yamakawa. It is respectfully submitted that Yamakawa is not applicable to IC chips that have a thickness less than 0.5 mm, such as chips for RFID tags. Thus, it is respectfully submitted that the teachings of Yamakawa, either alone or together with the teachings of Usami, et al., would have neither disclosed nor would have suggested the presently claimed invention, including such feature of use of the temporary securing pin, and advantages thereof in that IC chips having a small thickness, of, e.g., 0.15 mm, with a relatively small height and width or, e.g., 0.4 mm, can be processed.

It is respectfully submitted that the additional teachings of the references as applied by the Examiner in the Office Action mailed November 20, 2008, would not have rectified the deficiencies of Usami, et al., and of Yamakawa, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

In connection with claims 27, 28 and 31, Moskowitz, et al. discloses a radio frequency circuit and memory in a thin flexible package, used as a radio frequency tag. The radio frequency tag includes a semiconductor circuit that has logic, memory and radio frequency circuits, the semiconductor being mounted on a substrate and being capable of receiving a RF signal through an antennae that is electrically connected to the semiconductor through connections on the semiconductor. The elements of the package are placed adjacent to one another, that is, they are not stacked. See column 3, lines 9-20. Note also from column 3, lines 65, through column 4, line 10, disclosing, inter alia, the antenna of the tag, manufactured as an integral part of the substrate. See column 5, lines 53-59 of this patent.

Even assuming, arguendo, that the teachings of Moskowitz were properly combinable with the teachings of Usami, et al. and of Yamakawa, such combined teachings would have neither disclosed nor would have suggested the presently claimed invention, including, inter alia, the positional aligning step and step of securing the IC element with the temporary securing pin, and advantages of the present invention due thereto.

Green, et al. discloses methods of manufacturing radio frequency identification tags and labels, which include providing an RFID web stock having a plurality of recesses, each of the recesses containing an RFID chip, with a second web being provided having antennas spaced thereon. The RFID web stock is divided (severed, or separated) into a plurality of sections, each of the sections including one or more of the RFID chips. The pitch of the RFID sections is indexed from a high pitch density on the RFID web stock, to a relatively low pitch density on an RFID inlay stock. The sections are attached to a plurality of antennas in an automatic continuous process, so that each of the RFID chips is joined to one of the antennas to form an RFID inlay stock. Note paragraph [0021] on page 2 of Green, et al.; see also paragraph [0022] on page 2 thereof.

Even assuming, arguendo, that the teachings of Green, et al. were properly combinable with the teachings of Usami, et al., Yamakawa and Moskowitz, et al., as applied in paragraphs 15 and 16 on pages 9 and 10 of the Office Action mailed November 20, 2008, such combined teachings would have neither disclosed nor would have suggested the presently claimed invention, including, inter alia, the step of positionally aligning and the step of securing using a temporary securing pin, as in all of the present claims, and advantages thereof; and/or other features of the present invention as discussed previously, and advantages thereof.

In view of the foregoing comments and amendments, and particularly in view of the concurrently filed RCE Transmittal, entry of the present amendments, and reconsideration and allowance of all claims pending in the above-identified application, are respectfully requested.

To the extent necessary, Applicants hereby petition for an extension of time under 37 CFR 1.136. Kindly charge any shortage of fees due in connection with the filing of this paper, including any extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Account No. 01-2135 (case 1204.46401X00), and please credit any overpayments to such Deposit Account.

Respectfully submitted,

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